8.   What are three applications of multiplexers?

_____

_____

_____

9.   Name an application of demultiplexers.

_____

10.   How many control lines are needed for a 16 input multiplexer?

_____

In this lab exercise you will begin your study of MSI circuits. In this lab exercise you will also study the 4-line to 10-line decoder. This circuit is often used as a BCD to decimal decoder. It can also be used as a decoder for any number of binary inputs less than four such as 3-line to 8-line decoders and 2-line to 4-line decoders.

LAB EXERCISE 9.1
Decoders
Objectives

LD-2 Logic Designer

74LS42 4-Line to 10-Line Decoder

Jumper Wires
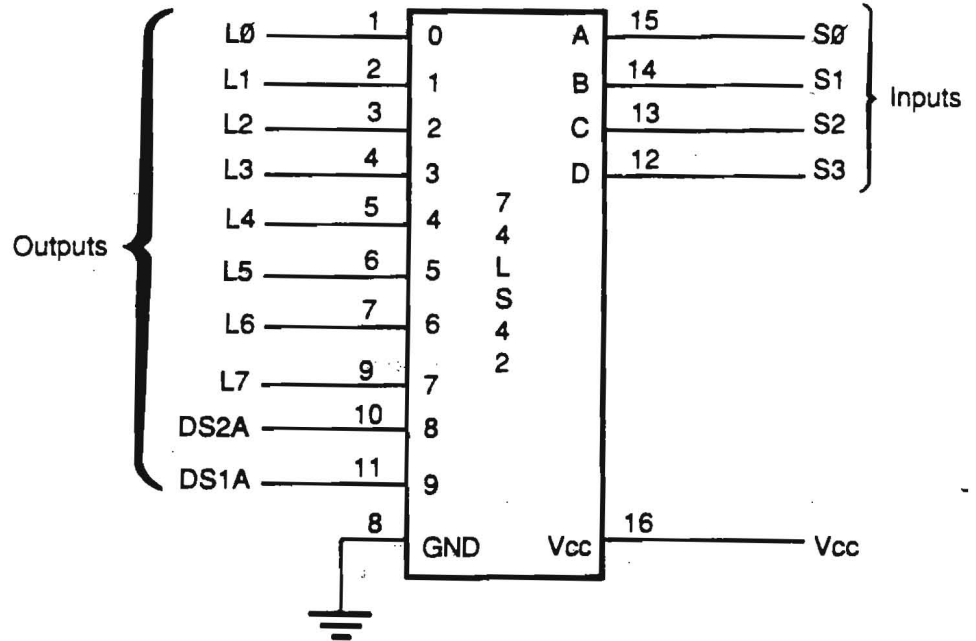
TTL Data Book

Materials

1.   Wire DS1 DE and DS2 DE to 5 VDC. Now wire the circuit shown in Figure 9-12. This is the circuit for a BCD/DEC decoder.

Procedure

FIGURE 9-12. BCD/DEC Decoder.

2. Place S0-S4 to LO. Turn on power. D1 and L1-L7 should light. DS1 and DS2 should show a count of 1.

3. Use S0-S3 as binary inputs. The LEDs L0-L7 are the decoded decimal outputs 0-7. DS2 is the 8 output and DS1 is the 9 output. Observe the circuit's operation and record your observations.

4. Now use S0-S2 as inputs and L0-L7 as the decoded outputs. This circuit is a 3-line to 8-line decoder.

5. Leave this circuit connected while you answer the following questions.

Questions

1. What happens to the outputs when a count greater than nine is entered onto the binary input lines?

_____

_____

2.   What type of circuit could you use to tell that an invalid input had been entered on the S0-S3 inputs?

_____

_____

3.   What type of circuit would you need to use to detect invalid inputs for the 3-line to 8-line decoder?

_____

_____

4.   Are the outputs of the 74LS42 LO true or HI true?

_____

5.   The LD-2 has an internal display driver so that the outputs of the 74LS42 are driving a TTL load and not a directly connected LED. Can the 74LS42 be used to drive an LED indicator directly? Explain your answer.

_____

_____

_____

In this lab exercise you will investigate the use of the 7447 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS. You will also learn about the use of seven-segment displays. You will study implementing simple displays.

LAB EXERCISE 9.2
Decoder/Drivers

Objectives

Materials

LD-2 Logic Designer

7447 BCD-TO-7-Segment Decoders/Drivers

TTL 312 Common-Anode 7-Segment Display

Jumper Wires

330 Ohm Resistors (7)

TTL Data Book

Procedure   1.   You will study the seven-segment LED display in the first part of this lab.   Place the TTL 312 onto the LD-s breadboard.

2.   Wire pin 14 to +5 VDC.   Connect one end of a 330 ohm to ground and use the other end to determine and record the basing diagram for the TTL 312.   No connection is made for pins 4,5 and 12.   Notice that the TTL 312 is a common anode display and that 7-segment displays are also available in a common cathode configuration.   Also note that the display segments are labeled clock-wise from the top as a-f.   The seventh segment is labeled as g and is the cross segment.   Many of these displays have left and right decimal points.   Some have the ability to display a leading minus sign.   Seven-segment displays are often used to form small arrays of decimal digits.   The display implemented here is a single digit decimal display.   A full digit decimal display can display any number 0-9.   A half-digit can only display a blank or a one.   Simple seven-segment displays can be made using LCD technology as well as LED technology.

3.   Wire the circuit shown in Figure 9-13.

FIGURE 9-13. BCD/7-Segment Decoder.

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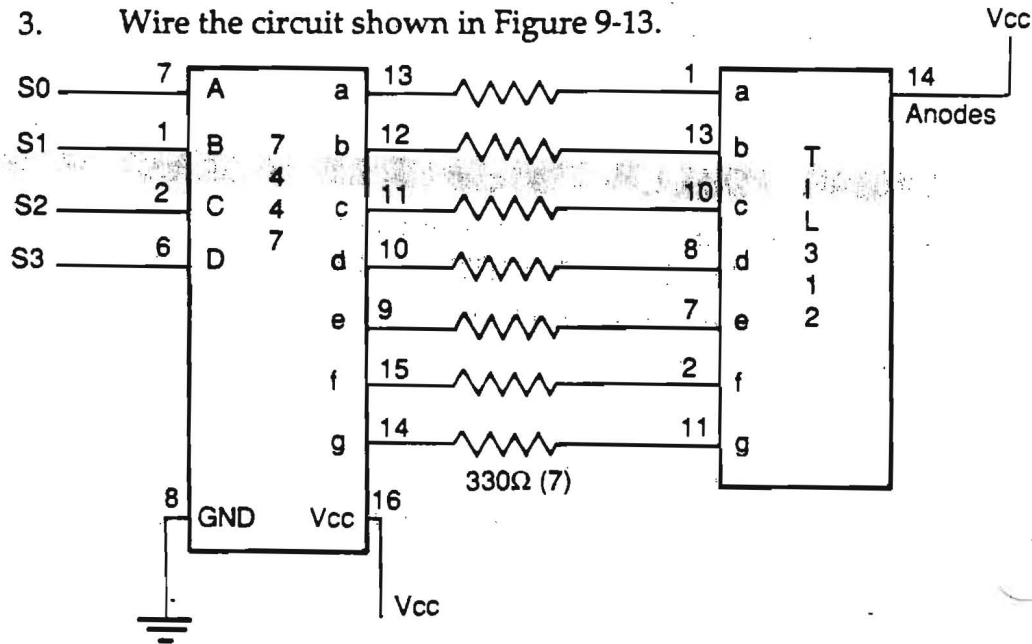
4. Turn S0-S3 to LO. D1 should light and a zero should be shown in the 7-segment display. Use S0-S3 as the A-D inputs and the display as the output. Observe and record the operation of this circuit. Compare this display circuit to the one used on the LD-2 and note differences.

5. Leave this circuit connected while you answer the following questions.

1. Is the display clear? How could this be improved?

Questions

_____

_____

2. What is the purpose of the 330 ohm resistors?

_____

3. What count is displayed when the TTL 312 consumes the greatest power ?

_____

4. What input is required to blank the display?

_____

The purpose of this lab exercise is to investigate encoders. You will study the 74LS148 eight-line-to-three-line encoder. This type of encoder is also known as an octal encoder. It could be used to encode an octal keypad or to convert octal to binary.

LAB EXERCISE 9.3
Encoders

Objectives

LD-2 Logic Designer

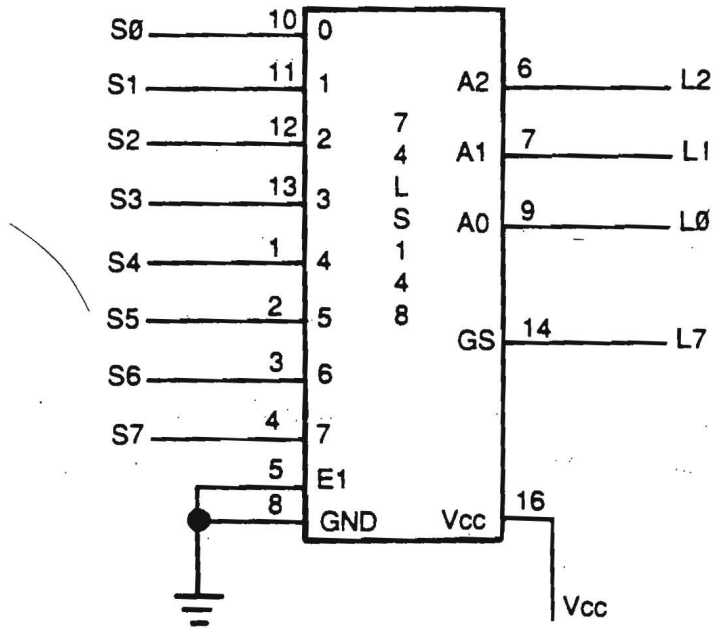**Materials**

74LS148 8-Line to 3-Line Priority Encoder

Jumper Wires

TTL Data Book

Procedure   1.   Place the 74LS148 onto the LD-2 breadboard. Connect power and ground to the 74LS148.

2.   Wire the circuit shown in Figure 9-14. This is the 8-line to 3-line encoder.

FIGURE 9-14. 8-Line to 3-Line Encoder.

3.   Place S0-S7 to HI. Turn on power. D1 and L0-L2 will light.

4.   Use S0-S7 as inputs and L0-L3 and L7 as outputs. Observe and record the operation of this circuit. Pay attention to what happens when more than one input is LO.

5.   Leave this circuit connected and answer the following questions.

Questions   1.   Are the inputs to the 74LS148 LO true or HI true?

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2.   Are the outputs used in this experiment LO true or HI true?

_____

3.   Explain what is meant by a priority encoder?

_____

4.   How can you tell the difference between a zero input and no input?

_____

_____

In this lab exercise you will study digital multiplexers. The 74LS153 4-line to 1-line data selector/ multiplexer will be studied.   A multiplexer can be used as a data selector or for parallel to serial conversion.   A multiplexer can also be used to implement logic functions.   The following lab exercise will familiarize you with the operation of the 4-line to 1-line multiplexer.

LD-2 Logic Designer

74LS153 4-Line to 1-Line Data Selectors/Multiplexers

Jumper Wires

TTL Data Book

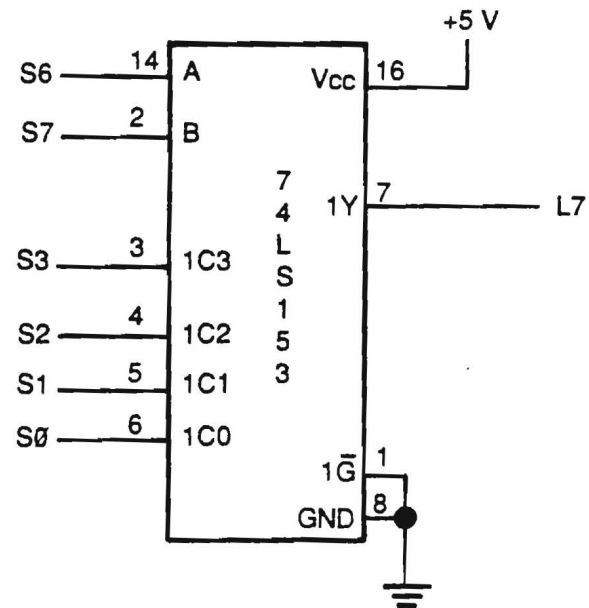**LAB EXERCISE 9.4**
Digital Multiplexers

Objectives

Materials

Procedure

1.   Place the 74LS153 on the LD-2 breadboard.   Wire power and ground to the circuit.

2.   Wire the circuit shown in Figure 9-15.   This circuit is a simple multiplexer.

FIGURE 9-15. Simple
Multiplexer.

3. Place S0-S3, S6 and S7 to LO. Turn on power. D1 should light.

4. Use S0-S3 as the data inputs, S6 and S7 as the select inputs and L7 as the output. Observe and record the operation of this circuit.

5. In this part of the experiment you will use the 74153 to implement a logic function. You will implement the logical AND function. To do this place S3 to HI and S0-S2 to LO.

6. Use S6 and S7 as the A and B inputs and observe the output on L7. Verify the truth table for this circuit.

7. Leave this circuit connected while you answer the following questions.

Questions   Explain the operation of the 4-line to 1-line multiplexer.

_____

_____

_____

2. How would you implement the logical EXNOR using a 74LS153?

_____

_____

_____

In this lab exercise you will study demultiplexers. Demultiplexers or data distributors are used extensively in digital computers. You will study the 74LS138 3-line to 8-line decoders/demultiplexers. This can be used as an address decoder for memory circuits or as a demultiplexer.

Objectives

LD-2 Logic Designer

74LS138 3-Line to 8-Line Decoders/Demultiplexers

Jumper Wires

TTL Data Book

Materials

1. Place the 74LS138 on the LD-2 breadboard. Wire power and ground to this circuit.

Procedure

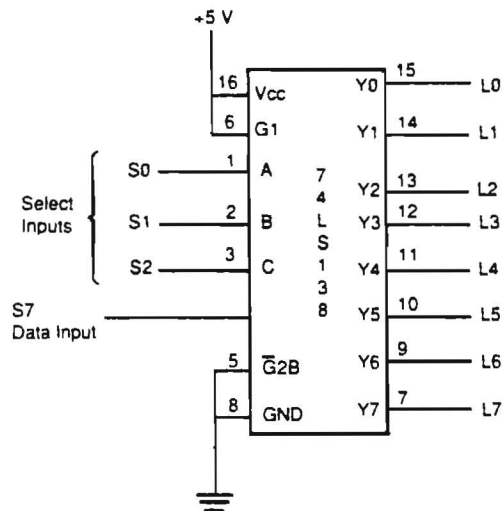2. Wire the simple demultiplexer circuit shown in Figure 9-16.

FIGURE 9-16. Simple Demultiplexer.

3. This circuit is a basic decoder circuit with additional gating for enabling the circuitry. Any decoder with one or more enable inputs can be used as a demultiplexer. Use S0- S2 as the select inputs, S7 as the data input and L0-L7 as the outputs. Observe the circuit operation and record your observations. Pay attention to the state of unselected outputs.

4. Leave this circuit assembled as you answer the following questions.

Questions

1. Since the demultiplexer is the inverse function of the multiplexer, could the 74LS138 be used for serial to parallel conversion?

_____

_____

2. What type of circuit is a demultiplexer made from?

_____